

THIN STACKED PACKAGE AND MANUFACTURING METHOD THEREOF

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to semiconductor devices and method for manufacturing the same, and more particularly to stackable structures for semiconductor integrated circuit packages and method for manufacturing the packages.

2. Description of the Related Arts

In general, semiconductor dies or chips are individually packaged for use in plastic or ceramic packages. A plurality of outer leads protruding from the package body are soldered on a supporting substrate such as a printed circuit board, or inserted into a socket. These packages, especially the packages inserted into the socket, have a large mounting area occupied on the printed circuit board.

The printed circuit board is being developed toward a smaller size and a higher density, and thereby requires a higher-density packaging technique. Therefore, a multichip module (MCM) or multichip package (MCP) capable of supporting several chips on a single package, has been developed.

The MCM or the MCP decreases the time delay between the chips, the electrical noise, and the crosstalk. Further, the MCM can employ much larger-sized chips, increase the number of I/O leads, and improve package mounting density to the substrate.

However, the above-described MCM has several drawbacks. Bare silicon chips for MCM cannot be tested before the chips are packaged. And, any one chip that is defective causes the entire module to fail when tested. Thus, the MCM is faced with poor yields and little chance of rework. In addition, MCM technology
5 does not permit burn-in of bare silicon chips; burn-in must be done at the module level.

A stacked package has been introduced as an alternative to the MCM. The stacked package not only reduces its overall size, but also allows for chip-level tests or burn-in before packaging. These three-dimensional stacked packages are
10 disclosed in, for example, U.S. Patent Nos. 5,138,438, 5,172,303, 5,198,888, and 4,763,188. Since the stacked package can improve the mounting density to the substrate and connecting density between the packages, it is applicable in a super computer and a large-scale cache memory.

However, since individual packages used in the stacking structure are much
15 thicker than the individual chips, the overall thickness of the stacked package increases considerably. It is therefore desirable to reduce the thickness of the individual packages and thereby realize thinner stacked packages.

Moreover, in the prior art stacked package structures it was necessary to deform or bend the package leads in order to interconnect upper and lower
20 packages, and this reduced the yield of the stacked package. For example, the outer leads of an upper package are typically connected to the outer leads of a lower package, or each of the outer leads of a plurality of packages are provided with a hole and the packages are stacked on a frame which includes a plurality of pins. The packages are stacked by maneuvering the packages so that the leads are
25 aligned with the plurality of pins.

SUMMARY OF THE INVENTION

According to the present invention compact semiconductor stacked packages are provided. According to another aspect of the invention, testing of the
30 individual packages of the stacked package can be performed. The invention

permits increased yields of the stacked package by eliminating additional leads deformation and/or treatment.

According to the present invention a stacked package is formed by stacking a plurality of semiconductor device packages, each package comprising a plurality of leads including inner leads having a predetermined thickness, and connection terminals having a thickness less than said predetermined thickness, a semiconductor chip electrically connected to the connection terminals, a package body encapsulating the semiconductor chip, the inner leads and the connection terminals, said package bodies having a thickness such that an upper and a lower surfaces of the inner leads is exposed. Herein each of the packages is stacked on another package by electrically connecting the exposed upper and lower surfaces of the inner leads with each other.

A lowermost package further comprises a plurality of outer leads integrated with the inner leads, said outer leads protruding from the package body and bent to be mounted on an external printed circuit board. The connection terminals are formed by etching a surface of the terminal ends of the inner leads. The semiconductor chip is electrically connected to the connection terminals of the inner leads by a metal wire and a depth of etching is greater than a wire loop height so that the metal wire is embedded by the molded package body. The metal wire is wedge-bonded to the semiconductor chip and the connection terminals of the inner leads, respectively. Alternatively, the semiconductor chip is electrically connected to the connection terminals of the inner leads by metal bumps. The exposed upper and lower surfaces of the inner leads and the surfaces of the outer leads are plated with a Sn-Pb alloy.

In another aspect of the present invention, a method is provided for manufacturing stacked packages by stacking a plurality of semiconductor device packages, said method comprising: preparing lead frames, each lead frame including: a chip receiving cavity; a plurality of inner leads having a thickness; a plurality of connection terminals having a smaller thickness less than that of the inner leads; a plurality of outer leads integrated with the inner leads; dam bars; tie bars; and a side frame; supporting a semiconductor chip; connecting the

semiconductor chip to the connection terminals; forming a package body by encapsulating the semiconductor chip, the inner leads, and the connection terminals and limiting a thickness of the package body by an amount which is sufficient to avoid covering the upper and lower surfaces of the inner leads;
5 removing dam bars from the side frame; separating packages from the lead frame; and forming a stacked package by stacking a plurality of the packages. Herein, each of the packages is stacked on another package by electrically connecting the exposed surfaces of the inner leads of one package to the exposed upper surfaces of the inner leads of another package.

10 According to another aspect of the present invention a semiconductor chip and package structure is provided which includes a semiconductor chip having a plurality of electrode pads, a plurality of electrically conductive leads, each having an inner end and an outer end, with the inner end of each lead being coupled to an associated electrode pad.

15 A housing is provided encapsulating the semiconductor chip and a portion of each of the leads, the housing having an upper surface, a lower surface and a thickness, wherein a portion of the leads have a thickness sufficient to expose an upper surface and a lower surface of each lead at the upper and lower surfaces, respectively, of the housing.

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BRIEF DESCRIPTION OF THE DRAWINGS

The various features and advantages of the present invention will be readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals
25 designate like structural elements, and, in which:

FIG. 1 is a plan view of a semiconductor device package according to a first embodiment of the present invention;

FIG. 2 is a cross-sectional view, taken along the line 2-2 of FIG. 1, of the semiconductor device package having outer leads bent in a gull wing shape;

FIG. 3 is a cross-sectional view of another semiconductor device package lacking outer leads according to the first embodiment of the present invention;

FIG. 4 is a flow chart illustrating a method for manufacturing the semiconductor device packages according to the first embodiment of the present invention;

FIGs. 5 through 12 illustrate each step of the manufacturing method of FIG. 4;

FIG. 5 is a perspective view of a lead frame having an adhesive tape attached thereto;

FIG. 6 is a perspective view of the lead frame having a semiconductor chip attached thereon;

FIG. 7 is a perspective view showing wire bonding;

FIG. 8 is a perspective view of a molded package body;

FIG. 9 is a perspective view showing a removal of the adhesive tape;

FIG. 10 is a perspective view showing the structure after removal of the dam bars;

FIG. 11 is a perspective view showing the semiconductor device package of FIG. 2 separated from the lead frame by cutting the outer leads and the tie bars; and

FIG. 12 is a perspective view showing semiconductor device package of FIG. 3 separated from the lead frame by cutting the inner leads and the tie bars;

FIG. 13 is a perspective view of a stacked package formed by stacking a plurality of the semiconductor device packages of the first embodiment;

FIG. 14 is a cross-sectional view of a semiconductor device package having outer leads to be bent in gull wing type according to a second embodiment of the present invention;

FIG. 15 is a cross-sectional view of another semiconductor device package lacking outer leads according to the second embodiment of the present invention;

FIG. 16 is a cross-sectional view of a stacked package which is formed by stacking a plurality of the semiconductor device packages of the second embodiment;

FIG. 17 is a cross-sectional view of a semiconductor device package having outer leads bent in a gull wing shape according to a third embodiment of the present invention;

FIG. 18 is a cross-sectional view of another semiconductor device package lacking outer leads according to the third embodiment of the present invention;

FIG. 19 is a flow chart illustrating a manufacturing method of the semiconductor device packages according to the third embodiment of the present invention; and

FIG. 20 is a cross-sectional view of a stacked package which is formed by stacking a plurality of the semiconductor device packages of the third embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below with reference to the accompanying drawings.

FIG. 1 is a plan view of a semiconductor device package 60 according to a first embodiment of the present invention. FIG. 2 is a cross-sectional view, taken along the line 2-2 of FIG. 1, of the package having a plurality of outer leads protruding from the package body and bent in a gull-wing shape.

Referring to FIGs. 1 and 2, the semiconductor device package 60 comprises a semiconductor chip 10, a plurality of leads 21 electrically connected to the semiconductor chip 10 via a metal wire 40, and a package body 50 encapsulating the semiconductor chip 10 and the metal wire 40 with a resin compound. For clarity, FIG. 1 shows only a partially completed package body 50 in order to illustrate leads 21, semiconductor chip 10 and metal wires 40.

The semiconductor chip 10 is an edge pad type chip having a plurality of bond pads 12 on opposite edges of its active surface. Although the illustrated embodiment uses an edge pad type chip 10, a center pad type chip, or a combined center and edge pad type of chip may be used in practicing the invention.

The leads 21 have inner leads 22 which are embedded in the package body 50, and outer leads 24 which protrude from the package body 50. Each inner lead

22 is integral with the corresponding outer lead 24. The leads 21 are arranged along opposite two sides of the semiconductor chip 10 and spaced from the sides. The lead 21 has the same thickness as the overall thickness of the package body 50. The current embodiment uses dual-type leads. However, quad-type leads may be used as an alternative.

FIG. 2 shows the semiconductor device package 60 having the outer leads 24 protruding from the package body 50 and bent in a gull-wing shape. The bent portions of the outer leads 24 serve as external contacts to provide electrical connection to a printed circuit board. The upper surfaces of the inner leads 22 are exposed at the upper surfaces of the package body 50 and serve to provide electrical connection to the lower surfaces of the inner leads 22 of another semiconductor device package 60a illustrated in FIG. 3.

The lower surface of the semiconductor chip 10 is exposed to the lower surface of the package body 50. That is, the lower surface of the semiconductor chip 10 is coplanar to the lower surface of the package body 50. The exposure of the chip facilitates the dissipation of heat generated in the chip.

Connection terminals 22a of the inner leads 22 are half-etched. It is preferable that the depth of the half-etching is greater than the wire loop height.

To lower the wire loop height, the metal wires 40 are wedge-bonded to both the semiconductor chip 10 and the inner leads 22.

In an exemplary embodiment, the semiconductor chip 10 is $100\mu\text{m}$ thick and the wire 40 has a diameter of $25\mu\text{m}$. In this case, the thickness of the package can be reduced to $200\mu\text{m}$. Preferably, the inner leads are half-etched to have the same height ($100\mu\text{m}$) as the thickness of the semiconductor chip 10. If the metal wire 40 is connected to the electrode pads 12 and the connection terminals 22a by the wedge bonding method, it is possible to lower the wire loop height up to approximately $50\mu\text{m}$, that is, double of the diameter of the metal wire 40.

In an alternate embodiment, the metal wires 40 are wedge-bonded to the inner leads 22 and ball bonded to the semiconductor chip 10.

In this case, the wire loop height should be controlled within the depth of the half-etching of the leads.

In the semiconductor device package 60a as illustrated in FIGs. 3 and 12, the outer ends of the leads are flush with the edge of package 60a. Depending on the treatment of the outer leads 24, either the semiconductor device package 60 in FIG. 2 or the semiconductor device package 60a in FIG. 3 may be alternatively formed. Herein, inner leads 22 are exposed to the upper, the lower, and the side surfaces of the package body 50. The exposed upper and lower surfaces of the inner leads 22 serve to provide electrical connection to the exposed upper and lower surfaces of the inner leads 22 of other semiconductor device packages 60 or 60a in stacking the packages. The semiconductor device package 60 of FIG. 2 is disposed on the lowermost of the stacked package, and the semiconductor device packages 60a of FIG. 3 are successively stacked on the lowermost semiconductor device package 60 of FIG. 2.

FIG. 4 is a flow chart 80 illustrating a method for manufacturing the semiconductor device packages according to the first embodiment of the present invention. FIGs. 5 to 12 illustrate each step of the manufacturing method of FIG. 4, and FIG. 13 shows a stacked package formed by stacking a plurality of the semiconductor device packages.

FIGs. 5 to 11 illustrate a method for manufacturing the semiconductor device package 60 of FIG. 2, and FIGs. 5 to 10 and 12 illustrate a method for manufacturing the semiconductor device package 60a of FIG. 3. That is, FIGs. 5 to 10 are common steps in manufacturing the semiconductor device packages 60 and 60a.

Referring to FIG. 5, a lead frame 20 patterned by etching or stamping a lead frame material which is made of a copper (Cu) or an iron (Fe) alloy is prepared (step 81). The lead frame 20 comprises a chip receiving cavity 32, a plurality of leads 21, dam bars 23, tie bars 27, and a side frame 25. The leads 21 are arranged along opposite two sides of the chip receiving cavity 32 and spaced from the sides at a designated distance. The dam bars 23 are formed perpendicular to the leads 21 to partition the leads 21 into inner leads 22 and outer leads 24, and to block the flow of the molding resin during an encapsulating step. The tie bars 27 are formed on the sides opposite to the two sides on which the leads 21 are

formed. The leads 21, the dam bars 23, and the tie bars 27 are supported by a side frame 25.

Connection terminals 22a are formed on terminal ends of the inner leads 22, which lie adjacent to the chip receiving cavity 32, by half-etching the inner leads 22.

Although the current embodiment describes one lead frame 20 for receiving one semiconductor chip, a lead frame strip comprising a plurality of lead frame units may be preferably used.

An adhesive tape 30 is attached to the lower surface of the lead frame 20 (step 82). The adhesive tape 30 serves to support and affix semiconductor chip 10 in cavity 32 and to prevent the overflow of the molding resin into the space between the dam bars 23 and the side frame 25 in an encapsulating step which may be a potting method.

FIG. 6 shows the step 83 of attaching a semiconductor chip 10. The semiconductor chip 10 is attached to the adhesive tape 30 in the chip receiving cavity 32 between the inner leads 22.

In order to manufacture the semiconductor device package having the same thickness as that of the lead frame 20, it is preferable to use the lead frame having a greater thickness of that of the semiconductor chip 10. For instance, where semiconductor chip 10 has a thickness of 100 μ m, a lead frame 25 preferably has a thickness twice that of the semiconductor chip 10, that is, approximately 200 μ m.

FIG. 7 shows a step 84 of electrically connecting the semiconductor chip 10 to the connection terminals 22a with a metal wire 40. Each connection terminal 22a of the inner lead 22 is wire-bonded to a corresponding electrode pad 12 of the semiconductor chip 10 via the metal wire 40 made of gold (Au) or aluminum (Al). To lower the wire loop height, the wedge-bonding method is employed. Alternatively, if wire loop height is controlled within the top of the package, the ball-bonding method on the electrode pads 12 of the semiconductor chip 10 and the wedge-bonding method on the connection terminals 22a may be used.

As shown in FIG. 8, the package body 50 is formed.(step 85) A liquid molding resin such as an epoxy molding compound (EMC) is injected and cured to

form the package body 50. Herein, the upper surfaces of the inner leads 22 and the tie bars 27 are exposed to the upper surface of the package body 50. In order to form the package body 50 having the same thickness as that of the lead frame 20, it is preferable to use the transfer molding method and the potting method. In the
5 transfer molding, the adhesive tape 30 serves as a lower mold while a flat upper mold is used. In the potting, the adhesive tape 30 prevents the leakage of the liquid resin.

FIG. 9 shows the completion of step 86 in which adhesive tape 30 has been removed from the lower surface of the lead frame 20. Thereby, the lower surfaces
10 of the inner leads 22 and the tie bars 27 are also exposed to the lower surface of the package body 50. FIG. 10 shows the completion of step of 87 in which dam bars 23 have been removed.

The above-described series of steps are common processes for manufacturing the semiconductor device packages 60 and 60a of FIGs. 2 and 3,
15 respectively.

In order to manufacture the semiconductor device package 60 of FIG. 2, the following step is carried out. FIG. 11 shows a step 88 of cutting the outer leads 24 from the side frame 25 and bending the outer leads 24 to be mounted on a printed circuit board. For example, the outer leads 24 are bent in a gull wing shape. Then,
20 the tie bars 27 are cut from the side frame 25. Thereby, individual semiconductor device packages 60 shown in FIG. 2 are separated from the side frame 25 (step 89). A reference numeral 27a refers to a trace of the cut tie bar 27 on the side frame 25, and a reference numeral 21a refers to a trace of the cut outer lead 24 on the side frame 25.

25 Alternatively, in order to manufacture the semiconductor device package 60a of FIG. 3, the following step is carried out after removing the dam bars 23. FIG. 12 shows step 89 of separating individual semiconductor device packages 60a from the lead frame 20 by cutting the inner leads 22 from the outer leads 24 and by cutting the tie bars 27 from the side frame 25. The step of cutting the inner leads
30 22 and the step of cutting the tie bars 27 may be carried out simultaneously or sequentially.

After the step 87 of removing the dam bars 23, the exposed upper and lower surfaces of the inner leads 22 and the surfaces of the outer leads 24 can be plated with a Sn-Pb alloy. This plating improves the reliability of connections between the inner leads 22 of adjacent stacked packages as illustrated in the stacking of the packages 60 and 60a shown in FIG. 13; and improves the reliability of connections between outer leads 24 and an associated printed circuit boards. Prior to plating, it is preferable to carry out a deflashing step to remove the resin residues, i.e., flash from the surface of the outer leads 24. If the lead frame is pre-plated, the above-described plating and deflashing steps may be omitted.

- 10 Referring to FIG. 13, a stacked package 70 is formed by stacking a plurality of the manufactured semiconductor device packages 60 and 60a according to the first embodiment. The semiconductor device package 60 having the bent outer leads 24 is placed on a lowermost position, and a plurality of the semiconductor device packages 60a lacking outer leads are successively stacked thereon.
- 15 Although FIG. 13 depicts the stacked package 70 having one lowermost package 60 and three packages 60a, however, the stacked package 70 may comprise more than three packages 60a stacked thereon. The bent portions of the outer leads 24 of the lowermost package 60 serve as external contacts for mounting the stacked package 70 on a printed circuit board. The exposed upper and lower surfaces of
- 20 the inner leads 22 of the packages 60 and 60a serve as internal contacts for electrically connecting the individual semiconductor device packages 60 and 60a to other package 60 and 60a.

- The connection of the inner leads 22 between the semiconductor device packages 60 and 60a is described as follows. As described above, the Sn-Pb alloy
- 25 plating layer is formed on the upper and the lower surfaces of the inner leads 22, which are exposed to the upper and the lower surfaces of the package body 50. After stacking a plurality of the semiconductor device packages 60 and 60a, the exposed upper surfaces of the inner leads 22 of a lower package are electrically connected to the exposed lower surfaces of the inner leads 22 of an upper package
- 30 by the reflow soldering at the temperature of approximately 180°C or more.

Alternatively, in order to improve the adhesive strength between the inner leads 22, solder paste may be further used. After applying the solder paste on the exposed upper surfaces of the inner leads 22, a plurality of the packages 60, 60a are stacked and the inner leads 22 are electrically connected to each other by the reflow soldering. Herein, the solder paste is easily applied by the known screen printing method.

FIG. 14 shows a semiconductor device package 160 having outer leads 124 protruding from the package body 150 and bent in a gull wing shape according to a second embodiment of the present invention.

With reference to FIG. 14, the semiconductor device package 160 comprises a lead frame 120 including a lower lead frame 126 and an upper lead frame 128 attached to the lower lead frame 126. The upper lead frame 128 is formed on the lower lead frame 126 except for terminal ends of the lower lead frame 126 which will be the connection terminals 122a. Other elements of the package 160 are identical with the package 60 of the first embodiment, and therefore their detailed descriptions are omitted.

According to the current embodiment, the connection terminals 122a are formed without the half-etching of the inner leads 122, and thereby the number of the manufacturing steps of the lead frame 120 can be reduced. First, the lower lead frame material is prepared. The upper lead frame material having an opening for exposing the connection terminal portions of the lower lead frame is attached to the lower lead frame material to manufacture the lead frame material 120. For a lead frame made of iron (Fe) having a melting point of 1,430 to 1,540°C, the upper lead frame 128 is attached to the lower lead frame 126 by heating with the temperature of approximately 800 to 1,300°C at a designated pressure.

FIG. 15 shows a semiconductor device package 160a in which the outer leads 124 have been removed from the package body 150 of the semiconductor device package 160 of FIG. 14. Depending on the treatment of the outer leads 124, the semiconductor device package 160 in FIG. 14 or the semiconductor device package 160a in FIG. 15 may be alternatively formed. Herein, inner leads 122 are exposed to the upper, the lower, and the side surfaces of the package body 150.

The manufacturing method of the semiconductor device packages 160 and 160a using the lead frame 120 of the second embodiment is the same as that of the first embodiment, and therefore the detailed description is omitted.

5 As shown in FIG. 16, a stacked package 170 of a plurality of the semiconductor device packages 160 and 160a has the same configuration as the stacked package 70 of the first embodiment in FIG. 13. The semiconductor device package 160 having the bent outer leads 124 is placed on a lowermost position, and a plurality of the semiconductor device packages 160a lacking the outer leads are successively stacked thereon.

10 FIG. 17 shows a semiconductor device package 260 having outer leads 224 protruding from the package body 250 and bent in a gull wing shape according to a third embodiment of the present invention.

With reference to FIG. 17, the semiconductor device package 260 comprises a semiconductor chip 210 having a plurality of electrode pads 212 thereon, metal bumps 240 on the electrode pads 212, a plurality of leads 221, and a
15 package body 250 formed by encapsulating the chip 210, the metal bumps 240, and partially the leads 221 with a liquid molding resin.

The semiconductor chip 210 is an edge pad type chip having a plurality of the electrode pads 212 along two opposite edges of the active surface, and a metal
20 bump 240 is formed on each electrode pad 212 and connects the chip 210 to the leads 221. The metal bumps 240 may be formed by any of the well known plating or wire bonding methods.

The leads 221 comprise a plurality of inner leads 222 embedded in the package body 250, and a plurality of outer leads 224 protruding from the package
25 body 250. Each inner lead 222 is integral with the corresponding outer lead 224. Connection terminals 222a are formed by etching the upper and the lower surfaces of the terminal ends of the inner leads 222, so that the semiconductor chip 210 is placed below the connection terminals 222a. Herein, the lower surface of the semiconductor chip 210 is coplanar to that of the inner leads 222.

30 FIG. 18 shows a semiconductor device package 260a in which the outer leads 224 from the package body 250 of the semiconductor device package 260 of

FIG. 17 have been removed. Depending on the treatment of the outer leads 224, the semiconductor device package 260 in FIG. 17 or the semiconductor device package 260a in FIG. 18 may be alternatively formed. Herein, inner leads 222 are exposed to the upper, the lower, and the side surfaces of the package body 250.

5 After forming the package body 250 by encapsulating the semiconductor chip 210 and the inner leads 222 including the connection terminals 222a, the lower surface of the semiconductor chip 210 is exposed to the lower surface of the package body 250. The connection terminals 222a are formed by etching the upper and the lower surfaces of the terminal ends of the inner leads 222. Herein,
10 the lower surfaces are etched more deeply than the upper surfaces. This permits semiconductor chip 210 to be attached to the lower surface of the connection terminals 222a by the metal bumps 240 on the electrode pads 212, and the lower surface of the semiconductor chip 210 is exposed to the lower surface of the package body 250.

15 Where semiconductor chip 210 has a thickness of 100 μ m and metal bumps 240, attached to the connection terminals 222a, have a height of 50 μ m, the semiconductor device package 260 and 260a having a thickness of 200 μ m can be provided by using the lead frame which is 200 μ m thick. It is preferable to maintain the distance from the lower surface of the inner lead 222 to the lower
20 surface of the connection terminal 222a at approximately 150 μ m.

Like other embodiments, in stacking a plurality of the packages 260 and 260a, the semiconductor device package 260 in FIG. 17 is placed on a lowermost position, and a plurality of the semiconductor device packages 260a in FIG. 18 are successively stacked thereon.

25 FIG. 19 is a flow chart illustrating a method 90 for manufacturing the semiconductor device packages according to the third embodiment of the present invention. Referring to FIG. 19, the manufacturing method 90 starts with a step 91 of preparing the lead frame having the connection terminals of the inner leads to be bonded to the metal bumps of the semiconductor chip. The lead frame of the this
30 third embodiment may take the form of lead frame 20 of FIG. 5 except for the connection terminals.

In this third embodiment, the use of adhesive tape is unnecessary since the semiconductor chip is bonded to the lower surfaces of the connection terminals of the inner leads with the metal bumps 240 on the chip (step 92).

5 Next, the encapsulating step 93 is performed to create the package body by encapsulating the semiconductor chip, the inner leads and the connection terminals. As the encapsulating method, the known transfer molding method is preferably used. Alternatively, adhesive tape may be attached to the lower surface of the lead frame and the semiconductor chip and known potting methods used for the encapsulation step.

10 After the encapsulating step, the process for manufacturing the semiconductor device packages of the current embodiment is the same as that of the first embodiment. To manufacture the semiconductor device package 260 in FIG. 17, a step 94 of removing the dam bar, a step 95 of cutting the outer leads from the side frame and bending the outer leads to be mounted on an external
15 printed circuit board, and a step 96 of separating individual semiconductor device packages from the lead frame by cutting the tie bars are successively carried out.

 Alternatively, in order to manufacture the semiconductor device package 260a in FIG. 18, after the step 94 of removing the dam bars, a step 96a of separating individual semiconductor device packages by cutting the inner leads
20 from the outer leads and the tie bars from the side frame is carried out.

 FIG. 20 shows a stacked package 270 formed by stacking a plurality of the semiconductor device packages 260 and 260a according to the third embodiment. Except for the connection terminals 222a of the inner leads 222 bonded to the semiconductor chip 210 with the metal bumps 240 on the chip 210, the stacked
25 package 270 has the same configuration as the stacked package 70 of the first embodiment.

 Although the present invention describes the stacked package by stacking one lowermost package having the outer leads bent in a gull wing shape, and a plurality of the packages lacking outer leads stacked thereon, the stacked package
30 may be formed by stacking only a plurality of the packages having the outer leads, or by stacking only a plurality of the packages lacking outer leads and attaching the

solder balls to the lower surfaces of the inner leads of the lowermost package to be mounted on the external printed circuit board.

Further, if necessary, various packages in different types of the above-described several embodiments of the present invention can be stacked to form a
5 stacked package.

According to the present invention, the package minimizes its overall thickness by making its thickness the same as that of the lead, that is the lead frame, and to thereby form thin stacked packages.

Since individual packages of the stacked package are interconnected to
10 each other by electrically connecting the exposed upper and the lower surfaces of the inner leads, it is easy to manufacture the stacked package. And, the stacked package can be mounted on the printed circuit board by electrically connecting the bent outer leads of the lowermost package to the printed circuit board. Therefore, the yield of the stacked package can be improved.

15 Further, since individual packages of the stacked package are manufactured by the conventional manufacturing method, additional equipment or steps are not required and the production costs are reduced.

Although preferred embodiments of the present invention have been described in detail hereinabove, it should be understood that many variations
20 and/or modifications of the basic inventive concepts herein taught still fall within the spirit and scope of the present invention as defined in the appended claims.